

Disclosure AUS8-2000-0753

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Required fields are marked with the asterisk (*) and must be filled in to complete the form .

Summary

Status	Under Evaluation
Processing Location	AUS
Functional Area	1A - SD - SERVER TECH/SP DEVELOPMENT (V. Lund)
Attorney/Patent Professional	Cas Salys/Austin/IBM
IDT Team	Roger Fuller/Austin/IBM
Submitted Date	07/24/2000 04:06:05 PM
Owning Division	SD
PVT Score	To calculate a PVT score, use the 'Calculate PVT' button.
Incentive Program	
Lab	
Technology Code	

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Technology Center 2100

Inventors with Lotus Notes IDs

Inventors: Daniel Dreps/Austin/IBM, Robert Williams/Rochester/IBM

Inventor Name > denotes primary contact	Inventor Serial	Div/Dept	Manager Serial	Manager Name
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Inventors without Lotus Notes IDs

IDT Selection

IDT Team: Roger Fuller/Austin/IBM	Attorney/Patent Professional: Cas Salys/Austin/IBM
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Response Due to IP&L : 08/24/2000

Main Idea

*Title of disclosure (in English)

Psuedo-Diferential Parallel Source Synchronous Bus

*Idea of disclosure

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

A method and apparatus are disclosed for extending a source synchronous bus to high frequency operation without conversion to a differential bus.

For details see the following files:



dreps_williams1.b



dreps_williams2.b



dreps_williams3.b



dreps_williams4.b



dreps_williams5.b

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

***Critical Questions (Questions 1 - 7 must be answered)**

Question 1

On what date was the invention workable? 07/24/2000 Please format the date as MM/DD/YYYY
(Workable means i.e. when you know that your design will solve the problem)

(2)

Pseudo-Differential Parallel Source Synchronous Bus

(A)



This design technique allows the extension of source synchronous buses to even higher frequency before conversion to differential buses must occur.

Single ended data bits require large amplitude single swings to manage adequate noise margin. Therefore single ended data bit buses run out of gas odd voltages decrease and line losses and bit rates increase.

Rambus, GTL, buses all are examples of low-swing single ended data buses with V_{ref} data receivers.

Example topology:

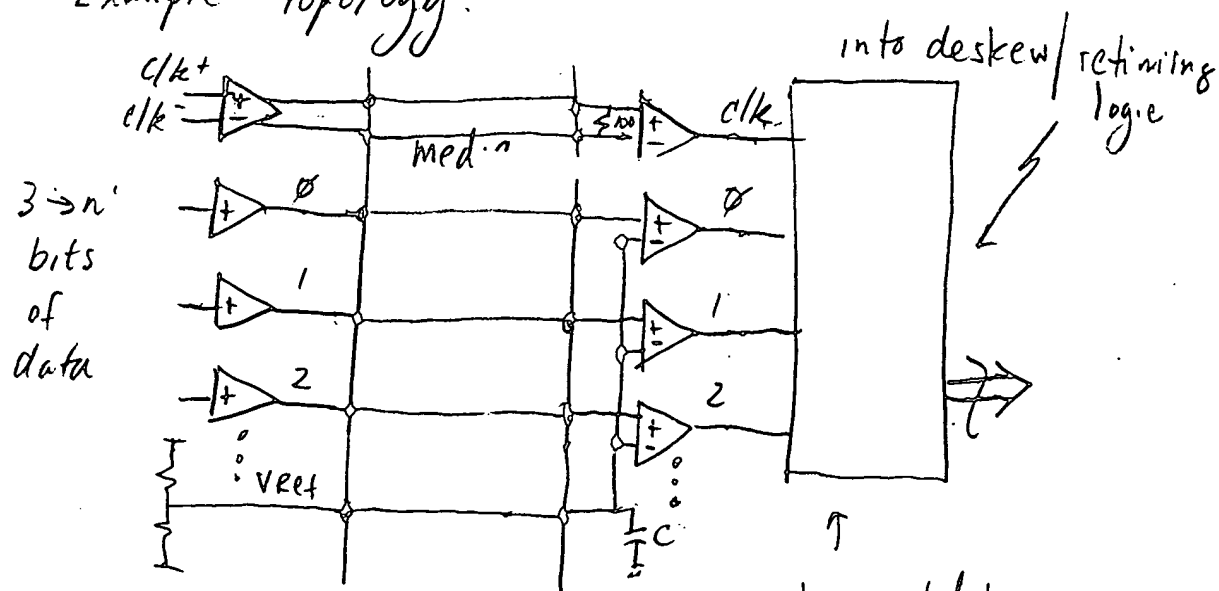


Figure 1

this could be
a RAMBUS/Elastic Interface/
STI/RID/Infraabrad Interface/
retimer deskew scheme.

Notice on the figure on page (A)
 an analog voltage is sent from the drive side to
 the RCVR side. The noise must be managed such
 that the DC to mid frequency ($< 50\text{MHz}$) noise
 generated from the drive side is transmitted to
 the rcvr. By doing this the noise tends to track
 the driver data bits. This results in a compensation
 or shift on vref when data bits shift up and down.
 The high frequency noise is rolled off on chip by C.

The alternative design approach is to generate
 the vref from the source synchronous clock.
 See the figure below:

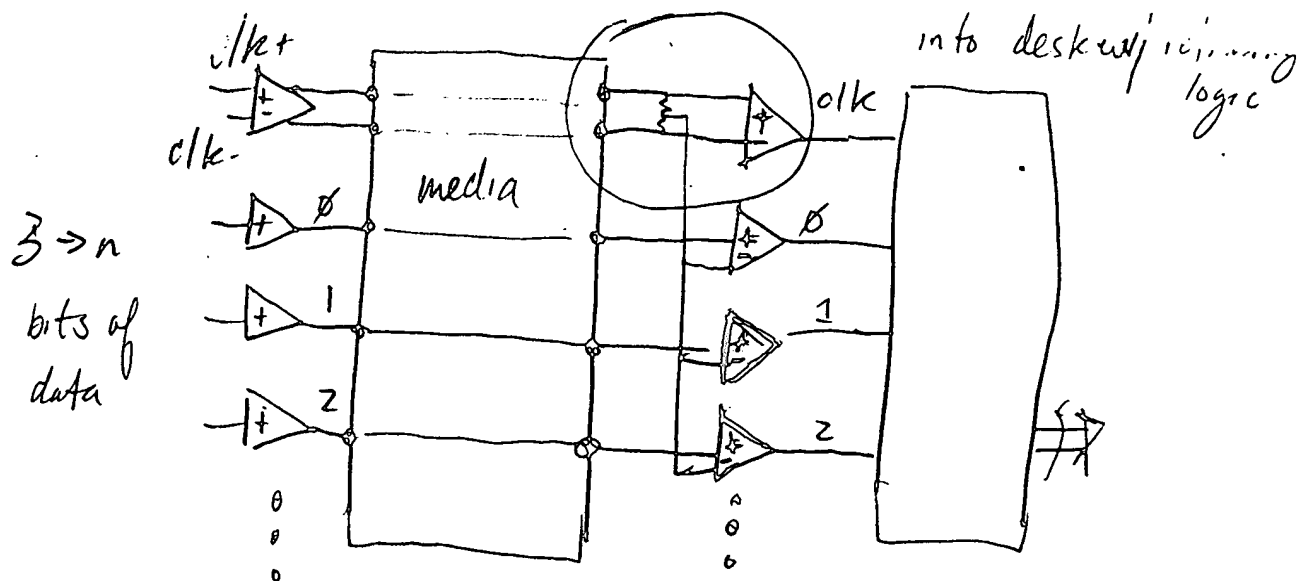


Figure 2

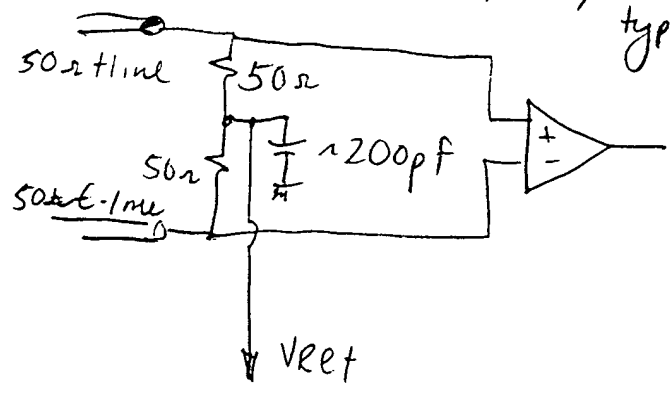


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Notice in figure 2 no additional V_{ref} pins are required, this means this design can be replaced with circuits that are the simple "vanilla" source synchronous design without a new package/board, etc.

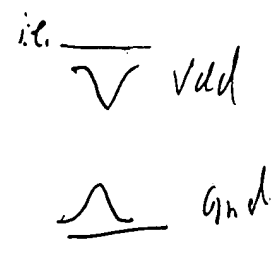
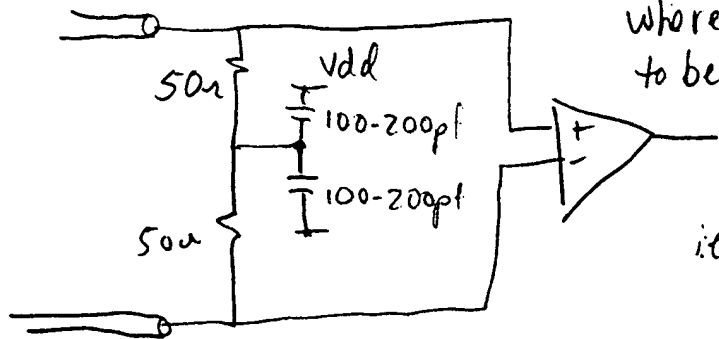
The exploded view of the bubble in figure 2 is shown below.

option A: (low-power, memory controller type designs < 20W)



option B:

+100 Watts
high power processors
where the noise tends
to be symmetric



Symmetric meaning V_{dd} droops at ~ same rate as ground rises

Figure 2: implies the clock is of a push-pull type so as the common-mode voltage would be exactly the $V_{swing}/2$ if all were perfect. Hence also the data bits swing symmetrically around a $V_{dd}/2$ level. Since the clock receiver is terminated into a differential 100Ω ($50 + 50$) the common mode point is at the center of 50Ω resistors and this is also what can be filtered to be V_{ref} .

No special decoupling is needed compared to the analog approach except for the on-chip filtering as shown in option A, B.

The DC and mid frequency and P/N mismatch of the clock/data driver is feed-forward to the receiver chip. The source-synchronous clock and data drivers are both of the exact same type as declared best for noise cancellation or tracking on the transmit side. (Better Common Mode Rejection)

The data/clock receivers should be designed such that they are identical or at least have similar delay and common-mode range. This results in shifts where noise events cause phase shifts on the receiver side to be common-mode out.

The net result is still a single ended bus where the Vref for the receiver moves in the directions to maximize noise margin as noise events occur.

This approach allows migratability with non-Vref'd packages/boards.

This approach extends the single ended bus bit rates

This approach is compatible with terminated, dynamic clamp, equalizing receivers.

This physical layer may be used in front of various retiming/deskew schemes.

This approach can be used and will be used in IBM's powerPC design.